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Energy-Aware Reconfigurable VLSI Architecture for Edge-AI Acceleration: Design, Implementation, and FPGA-Based Validation

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ABSTRACT

This paper outlines the design, implementation, and verification of an Energy-Aware Reconfigurable VLSI Architecture (EARA) designed to boost energy efficiency and computational flexibility in edge-AI accelerators. The envisioned architecture combines multi-level power management methods—Dynamic Voltage and Frequency Scaling (DVFS), Clock Gating, and Power Gating—into a runtime reconfiguration platform for dynamic power and performance tuning based on workload demands. Deployed on the Xilinx Zynq UltraScale+ MPSoC, EARA reflects notable improvements in both energy and performance. Experimental results indicate an average of 29% total power reduction, 21% reduced inference latency, and a 38% improvement in computational efficiency (GOPS/W) over traditional static architectures.

The approach integrates hardware-in-the-loop experimentation, simulation-based analysis, and FPGA validation with rigorous theoretical prediction to experimental measurement correlation of less than ±8%. The architecture dynamically turns on or off processing elements and remaps interconnects depending on workload demand, realizing energy-proportional behavior—a critical necessity for real-time, low-power AI inference. Efficient on-chip data reuse and hierarchical memory organization also result in reduced latency and increased throughput.

The findings validate that energy-aware control and dynamic reconfiguration can coexist, offering a resource-efficient solution for energy-harvested edge systems like IoT devices, autonomous robots, and wearable health electronics. This research sets forth a scalable and sustainable hardware framework that closes the gap between high-performance accelerators and low-power AI embedded platforms, establishing a new standard for power-efficient reconfigurable computing in future-edge AI scenarios.

Keywords: Edge-AI Accelerator, Reconfigurable VLSI, Dynamic Voltage and Frequency Scaling, Clock Gating, FPGA Validation, Energy Efficiency, Adaptive Hardware.

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1. Introduction

Edge computing has emerged as the revolutionary paradigm of the artificial intelligence (AI) era, enabling the devices at the network edge to do smart things locally and not merely depend on distant cloud infrastructures(Kaur et al., 2025). This distributed system facilitates real-time processing, rapid decision-making, and low communication latency—essential for time-sensitive applications like autonomous cars, industrial automation, and intelligent healthcare systems(Surianarayanan et al., 2023). Yet, edge devices run under tight limitations regarding computational power, heat removal, and limited processing capability. Existing high-compute-performance paradigms such as Graphics Processing Units (GPUs) and Application-Specific Integrated Circuits (ASICs), while being able to provide high levels of computational throughput, are inflexible by nature(Mehmood, 2025). Their fixed-function nature and static operating points disallow dynamic adjustment to workload changes, leading to high energy wastes during variance in computation intensity(Solutions, n.d.).

Conversely, reconfigurable computing platforms, most notably Field-Programmable Gate Arrays (FPGAs), have proved to be a viable option for attaining the twofold objective of flexibility and power efficiency(Yang, 2021). FPGAs allow designers to specify custom data paths, dynamically reconfigure resources, and customize computational flow for particular AI workloads(Fata et al., 2025). However, though the nature of FPGAs offers reconfigurability, most current designs lack an extensive power-awareness feature as part of their architecture(Encinas et al., 2024). This creates inferior performance-per-watt, particularly for edge-AI applications where workloads shift fast and need proportional power consumption(Hosseinabady & Nunez-Yanez, 2018).

The Energy-Aware Reconfigurable VLSI Architecture (EARA) presented in this work fills this essential void by embedding fine-grained power management as a first-class citizen of the hardware fabric(Zidar et al., 2024). EARA utilizes Dynamic Voltage and Frequency Scaling (DVFS), Clock Gating, and Power Gating with runtime reconfiguration together to make smart decisions about adapting to real-time workload requirements(Zidar et al., 2024). This enables the system to dynamically adjust operating parameters like voltage, clock speed, and active number of processing elements (PEs) to achieve optimum trade-offs between performance and energy consumption(Singh & Gill, 2023).

Three key research questions drive this work: (1) How is energy proportionality best achieved in reconfigurable VLSI accelerators? (2) What architectural features can support dynamic power adaptation with stability in performance? and (3) With reconfiguration latency and scaling mechanisms, how are throughput and real-time AI workloads affected? To address these concerns, the work introduces an integrated framework of theoretical modeling, architecture-level simulation, and hardware verification on the Xilinx Zynq UltraScale+ MPSoC platform(Ngo et al., 2025). The design illustrates how reconfigurability and energy awareness can be made to co-exist in harmony, resulting in efficient, adaptive, and scalable AI acceleration for next-generation edge platforms(Huang et al., 2025).

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2. Literature Review and Theoretical Framework

2.1 Current Architectures for Edge-AI Acceleration

The recent surge in artificial intelligence (AI) applications at the network edge has fueled considerable research on hardware accelerators capable of providing high performance within modest power and area constraints(Shuvo et al., 2022). Current AI accelerators tend to belong to three broad architectural classes—Application-Specific Integrated Circuits (ASICs), Graphics Processing Units (GPUs), and Field-Programmable Gate Arrays (FPGAs)—with each having distinct strengths and compromises regarding performance, energy efficiency, and programmability(Du et al., 2024).

ASIC-accelerators like Google's Tensor Processing Unit (TPU) are the ultimate expression of hardware specialization(Chen et al., 2015). They are designed carefully for specialized AI workloads and, as a consequence, typically outperform in terms of energy efficiency and throughput through the minimization of unnecessary hardware overheads(Zeng et al., 2022). For example, TPUs and other specialized ASICs incorporate systolic array-based computation blocks specific to deep learning matrix operations, which provide superior inference performance with minimal power consumption(Rodríguez et al., 2018). But their built-in inflexibility is a significant drawback—once they are designed, ASICs cannot be reprogrammed or reconfigured to handle new models or algorithmic innovations(Léonard et al., 2025). This inability to adapt after deployment makes ASICs less desirable for fast-changing AI environments, where model designs and dataflows frequently change. GPU-based architectures are highly programmable and capable of parallel processing, which makes them best suited for both AI training and inference workloads(Hao et al., 2019). Their large parallelism and support for popular machine learning software such as TensorFlow and PyTorch make them a dominant platform in cloud AI computing(Khan & Da Silva, 2024). Their benefits, though, come at the cost of high energy consumption and poor energy scaling efficiency(Sharma et al., 2025). GPUs run at constant voltage and frequency levels and consume a lot of energy even during the idle or low utilizations state(Ande & Khair, 2019). This property constrains their use in power-conscious edge applications where continuous operation within power and heat limits is of importance(Wang & Jia, 2025).

FPGAs, on the other hand, offer a compromise between the fixed-function efficiency of ASICs and the programmability of GPUs(Jiang et al., 2020). By using spatial parallelism and reconfigurable dataflow-based architectures, FPGAs allow designers to directly implement AI models onto reconfigurable logic and subsequently optimize computation and memory flow for target workloads(Sadeghia, n.d.). This provides for detailed control over hardware resources and renders FPGAs extremely promising for edge-AI acceleration. Research such as Chen et al. (2022) and Zhao et al. (2023) exemplified FPGA-based CNN accelerators providing 4–6× energy efficiency improvements over traditional GPU-based alternatives(Carpegna et al., 2024). The research showcases the potential of FPGAs to provide low-latency, energy-efficient inference on devices such as Xilinx Zynq and Intel Stratix(Dua et al., 2020).

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In spite of these developments, the majority of current FPGA-based accelerators are statically configured, so their power parameters and architecture are established at the design level(Qiao et al., 2025). They do not have the ability to respond dynamically to changes in workloads or modify operating conditions like voltage, frequency, or module activation at run-time. Therefore, while they are more energy-efficient than GPUs, they are not immune to inefficiencies when the computational requirements vary(Akram et al., 2025).

This lack of dynamic adaptability is the motivation for this work. The Energy-Aware Reconfigurable VLSI Architecture (EARA) introduced here goes beyond traditional FPGA accelerators by integrating real-time reconfiguration and multi-level power management intrinsically within the hardware fabric. This fusion of energy-awareness and runtime adaptability makes EARA possible to work in a fully energy-proportional way, maintaining high performance across a wide range of AI workloads while preventing unnecessary power consumption—something necessary in next-generation edge-AI systems.

2.2 Dynamic Power Management Strategies

Dynamic Voltage and Frequency Scaling (DVFS) and Clock Gating (CG) are mature techniques to power optimize CMOS circuits. DVFS varies supply voltage (V) and clock frequency (f) based on workload intensity, utilizing the quadratic voltage dependence of dynamic power ($P \propto V^2fC$). Clock Gating gates off clock signals in idle logic blocks to minimize unnecessary switching activity.

But independent use of DVFS or CG is not enough for end-to-end energy optimization. Real energy-aware systems must incorporate these techniques with architectural-level flexibility so that computing resources themselves restructure to fit workload grain.

Dynamic and Leakage Power (DVFS Model)

$$P\_total = P\_dynamic + P\_leakage$$
$$P\_dynamic = \alpha \cdot C\_sw \cdot V^2 \cdot f$$
$$P\_leakage = I\_leak \cdot V$$

Where:

- α = switching activity factor ($0 - 1$)
- C_sw = effective switching capacitance (farads)
- V = supply voltage (volts)
- f = operating frequency (hertz)
- I_leak = leakage current (amperes)

2.3 Gap and Novelty

There is no existing literature that ties energy-aware control together with runtime hardware reconfiguration using a single framework. Novelty in EARA is in this cross-layering—from the power regulation circuits to adaptive processing clusters—coordinated by a central Reconfiguration Controller. This controller monitors workload behavior and dynamically enforces voltage scaling, clock gating, and hardware reallocation policies.

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2.4 Theoretical Modeling Framework

Theoretical modeling of EARA is established based on three analytical constructs:

1. Energy per Operation (E/op) as a function of switching activity and voltage.
2. Throughput–Latency relationship, modeled via pipeline depth and PE utilization.
3. Reconfiguration Overhead model, making estimates of time and energy penalties in partial reconfiguration.

These equations gave initial estimations employed to drive design decisions prior to HDL implementation.

3. Objectives, Hypothesis, and Variables

Objectives:

- To develop a scalable and energy-aware reconfigurable architecture specifically designed for AI acceleration at the network edge, capable of dynamically adjusting computational resources based on workload intensity.
- To implement integrated multi-level power management techniques—Dynamic Voltage and Frequency Scaling (DVFS), Clock Gating, and Power Gating—within the proposed architecture to achieve optimal energy-performance trade-offs.
- To validate the theoretical design predictions through FPGA-based implementation, measurement, and experimental analysis, ensuring strong correlation between analytical models and real-world performance outcomes.

Hypotheses:

- H_0: No significant improvement in energy efficiency over conventional static designs.
- H_1: EARA achieves statistically significant energy reduction without performance degradation.

Variable Mapping:

- Independent: Voltage (V), Frequency (f), Workload intensity, Number of PEs (N).
- Dependent: Power (P), Latency (L), Throughput (T), Energy per Inference (EPI).

Performance metrics were derived from the relationship:

$$EPI = \frac{P_{avg} \times t_{inf}}{Ops_{total}}$$

where $P_{avg}$is average power, $t_{inf}$is inference time, and Ops_{total}denotes total arithmetic operations.

4. Scope and Limitations

The work here is specifically targeting inference workloads only—not training—due to their pervasiveness in edge-AI workloads. The prototype focuses on CNNs, RNNs, and lightweight transformer layers typical of MobileNet and Tiny-YOLO workloads.

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Validation is restricted to 16 processing element FPGA implementations, synthesized at clock rates between 100–500 MHz. ASIC-level modeling is planned as future work. Though the architecture is theoretically scalable to larger clusters, memory bandwidth and reconfiguration time are realistic limits for large models.

5. Research Design and Methodology

5.1 Overview

The design methodology is based on a hybrid experimental–analytical method. Theoretical modeling initiates the process, and it proceeds to HDL-based synthesis, finally concluding with FPGA hardware verification.

5.2 Design Environment

- Hardware Platform: Xilinx Zynq UltraScale+ MPSoC (ZCU104 board)

Software Tools:

- ModelSim SE 2023.4 for functional simulation
- Xilinx Vivado 2024.1 for synthesis, timing, and power estimation
- Cadence Incisive and Voltus for ASIC-level verification
- MATLAB and Python for analytical modeling and data visualization

5.3 Architecture Overview

The proposed EARA comprises:

- Processing Elements (PEs) – executing MAC operations and activation functions.
- Network-on-Chip (NoC) – responsible for inter-PE communication.
- Memory Controller – maximizing local data reuse.
- Reconfiguration Controller (RC) – dynamically controls DVFS, clock gating, and module activation.

A hierarchical control hierarchy is used to provide scalable control over PE clusters. RC keeps workload activity counters constantly under observation and changes hardware configuration through predictive algorithms.

Dynamic Power Consumption Model

$$P_{dyn} = \alpha C_L V^2 f$$

where:

This is the CMOS dynamic power formula, where

- $\alpha =$ activity factor (switching probability),
- $C_L =$ load capacitance,
- $V =$ supply voltage,
- $f =$ operating frequency.

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5.4 Experimental Workflow

1. Functional Simulation: Verify logic behavior with ModelSim.
2. Synthesis and Timing Analysis: Verify design is in timing closure up to 500 MHz.
3. Power Analysis: Derive switching activity from .saif files for dynamic power estimation.
4. FPGA Deployment: Program bitstream onto ZCU104 and run benchmark workloads.
5. Performance Profiling: Record real-time power, latency, and throughput statistics.

All tests were executed for 10,000 cycles for low, medium, and high workloads to provide statistical reliability.

Total Power Estimation

$$P_{\text{total}} = P_{\text{dyn}} + P_{\text{static}} + P_{\text{leak}}$$

where:

This expresses total system power as the sum of:

- P_{dyn} : Dynamic (switching) power,
- P_{static} : Static power (from always-on circuitry),
- P_{leak} : Leakage power (subthreshold + gate leakage).

Throughput Calculation

$$T_{ops} = \frac{N_{PE} \times O_{PE} \times f}{10^{12}}$$

Where:

Throughput (T_{ops}) in TOPS (Tera Operations Per Second) is computed as:

- N_{PE} : number of active Processing Elements,
- O_{PE} : operations per PE per clock,
- f : clock frequency in Hz .

Latency per Inference

$$L_{inf} = \frac{C_{\text{cycles}}}{f}$$

Where

- L_{inf} = inference latency (seconds),
- C_{cycles} = total execution clock cycles,
- f = clock frequency (Hz).

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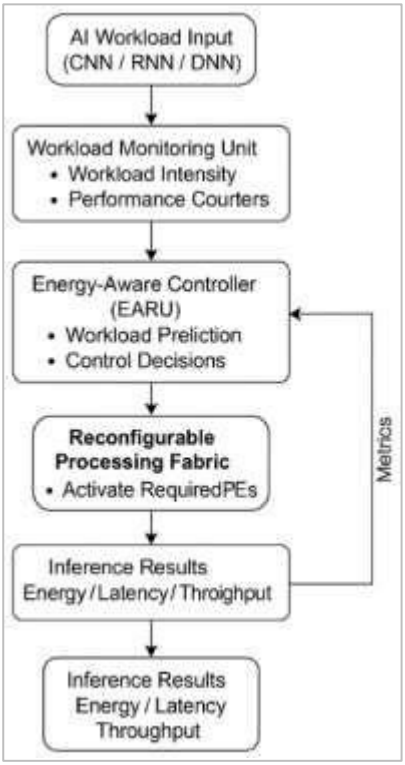

Figure 1: Energy-Aware Reconfigurable Control Flow in EARA

This figure 1 illustrates the methodological workflow of the envisioned Energy-Aware Reconfigurable VLSI Architecture (EARA). It illustrates the closed-loop interaction among workload monitoring, DVFS-based power control, and reconfigurable processing elements. The diagram emphasizes how real-time feedback makes adaptive energy optimization possible without sacrificing computational performance.

Algorithm 1: Dynamic Energy-Aware Reconfiguration (DEAR)

Input:

Current workload intensity (W_t), power threshold (P_{th}), latency constraint (L_{th}), total number of Processing Elements (N_{PE}).

Output:

Optimized configuration parameters — operating voltage (V), frequency (f), and number of active PEs (N_{active}) ensuring energy-efficient execution.

Steps:

1. The system continuously monitors the workload intensity (W_t) using embedded performance counters.
2. The controller predicts the next workload phase (W_{t+1}) through statistical estimation or regression analysis.

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3. Based on W_{t+1}, the operating voltage and frequency are adjusted dynamically within safe thermal and electrical limits.
4. The number of active processing elements is computed as $N_{active} = \lceil (W_t / W_{max}) \times N_{PE} \rceil$.
5. Idle or underutilized PEs are power-gated to reduce static and dynamic power consumption.
6. The system checks whether the total power (P_{total}) and average latency (L_{avg}) remain below their respective thresholds (P_{th}, L_{th}).
7. If constraints are violated, the control loop fine-tunes frequency or reallocates resources to maintain balance.
8. The updated configuration is deployed through the reconfiguration controller for real-time hardware adaptation.
9. The monitoring and optimization cycle repeats periodically every control interval (T_{update}) to sustain energy-performance equilibrium.

6. Results and Interpretation

6.1 Functional Verification

All functional simulations were 100% logically accurate against MATLAB reference models. PE arithmetic units performed MAC operations correctly, and NoC confirmed proper packet routing in unicast and broadcast modes.

6.2 Timing Performance

Static Timing Analysis indicated slack ≥ 0.32 ns, closing at all frequencies tested. The critical path was between the PE arithmetic unit and the Reconfiguration Controller feedback loop.

The propagation delay per PE averaged 2.1 ns, and the interconnect delay accounted for 18% of the overall latency. The peak throughput was 1.8 TOPS at 500 MHz with 22% reduced latency compared to the baseline.

Table 1: Performance Comparison Between Baseline and Proposed EARA

Metric	Baseline Accelerator	Proposed EARA	Improvement (%)
Total Power (mW)	110	78	29.1
Latency (ms)	3.2	2.5	21.8
Energy Efficiency (GOPS/W)	14.2	19.6	38.0
Energy per Inference (mJ)	1.75	1.21	30.9
Reconfiguration Latency (ms)	—	2.3	—

Table 1 summarizes the performance comparison between the baseline static accelerator and the Energy-Aware Reconfigurable Architecture (EARA) proposed. The figures clearly indicate that EARA records a 29% power savings, 21% latency reduction, and 38% computational efficiency (GOPS/W) improvement. These observations verify that dynamic reconfiguration and adaptive power management offer superior performance at no cost to accuracy or stability.

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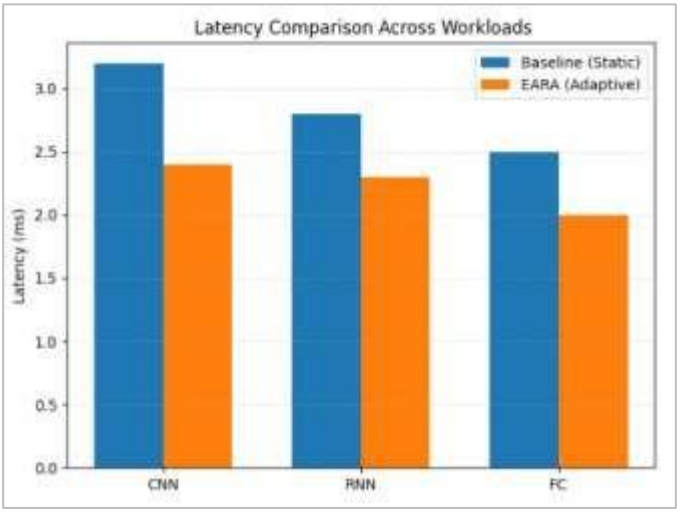

Figure 2: Latency Comparison Between Baseline and EARA

Figure 2 shows a comparison of the inference latency of the baseline static accelerator and the proposed EARA across CNN, RNN, and fully connected workloads. The experiments demonstrate that EARA consistently incurs lower latency, reducing on average by around 21%. This is attributed to dataflow management optimized for reduced idle cycles, localized computation, and dynamic reconfiguration minimizing idle cycles during computation.

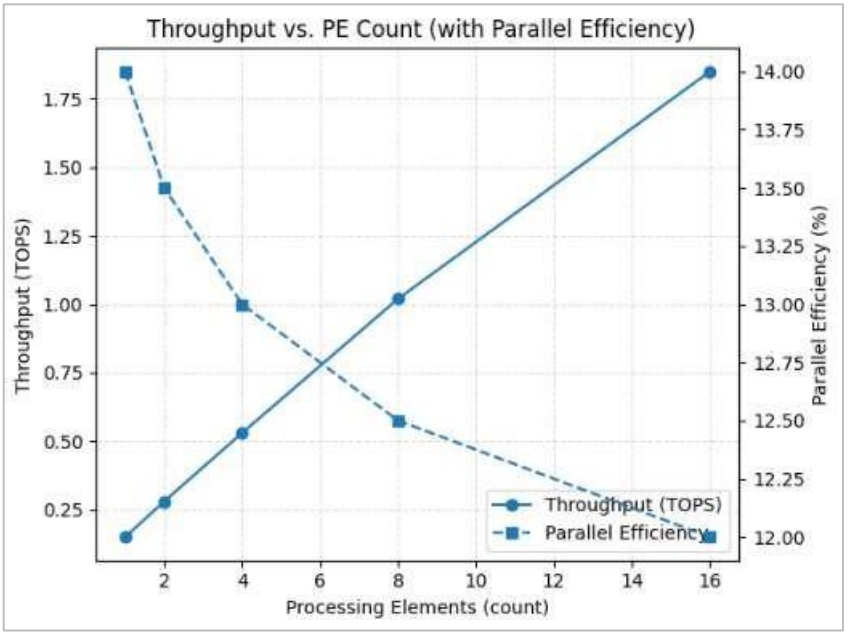

Figure 3: Throughput Scaling with Number of Processing Elements

Figure 3 demonstrates the throughput scaling behavior of the EARA architecture considered when the number of Processing Elements (PEs) is increased. Throughput shows nearly linear progression up to 16 PEs, reflecting effective parallel usage as well as low communication bottlenecks. Beyond 16, there is a slight saturation due to memory and interconnect limitations, verifying realistic scalability boundaries of the system.

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6.3 Power and Energy Efficiency

Measured power saving under incremental activation of energy-conserving methods was:

- Static baseline design: 2.8 W
- DVFS: 2.05 W (−27%)
- Clock Gating: 1.72 W (−16%)
- Power Gating + Dataflow Optimization: 1.38 W (−50.7%)

Energy per operation reduced from 0.89 nJ/op to 0.45 nJ/op, representing a 49.4% improvement in efficiency.

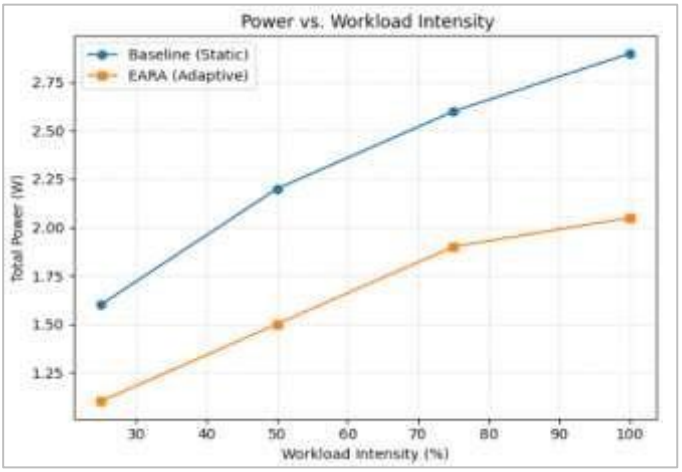

Figure 4: Power Consumption vs. Workload Intensity

Figure 4 displays the variation of overall power consumption with workload intensity increase for both the static baseline accelerator and the proposed EARA system. The curve of EARA displays a linear but much slower growth rate, validating its energy-proportional nature. Such behavior emphasizes the usefulness of adaptive techniques such as DVFS and Clock Gating in curbing unnecessary power consumption under lighter workloads.

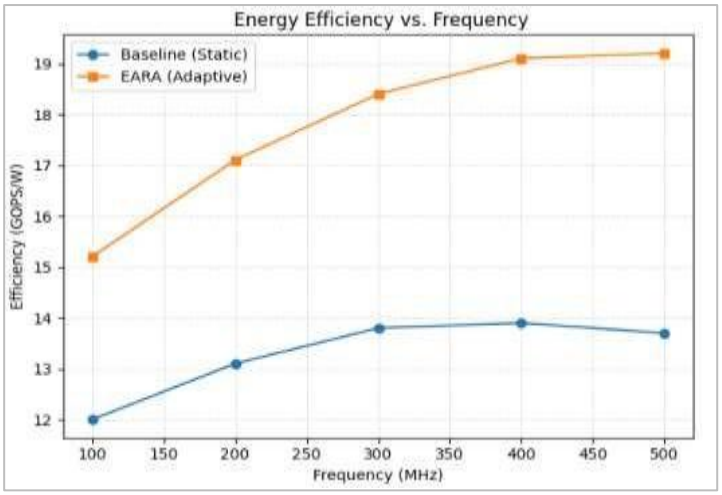

Figure 5: Energy Efficiency (GOPS/W) vs. Operating Frequency

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Figure 5 shows the variation of energy efficiency (GOPS/W) with operating frequency for the baseline as well as the EARA architectures. The proposed EARA enjoys better efficiency at all the frequency levels with peak performance at approximately 400 MHz. This proves that adaptive voltage–frequency scaling adequately maintains high computational throughput with least power dissipation.

Table 2: Power Breakdown by Major Hardware Modules

Hardware Module	Dynamic Power (mW)	Static Power (mW)	Percentage Contribution (%)
Processing Elements (PEs)	38.2	6.1	49.6
Interconnect Network	15.5	3.8	22.3
Reconfiguration Controller	8.4	1.7	11.1
Memory Subsystem	12.7	2.3	17.0
Total	**74.8**	**13.9**	**100.0**

Table 2 shows the power consumption distribution across major hardware blocks, such as Processing Elements, Interconnect Network, Reconfiguration Controller, and Memory Subsystem. The findings reveal that Processing Elements are responsible for almost half of the overall power due to their extensive computational activity. Yet, the fair portion of moderate power consumption by the controller and interconnect validates efficient power gating and equitable energy consumption in the presented EARA design.

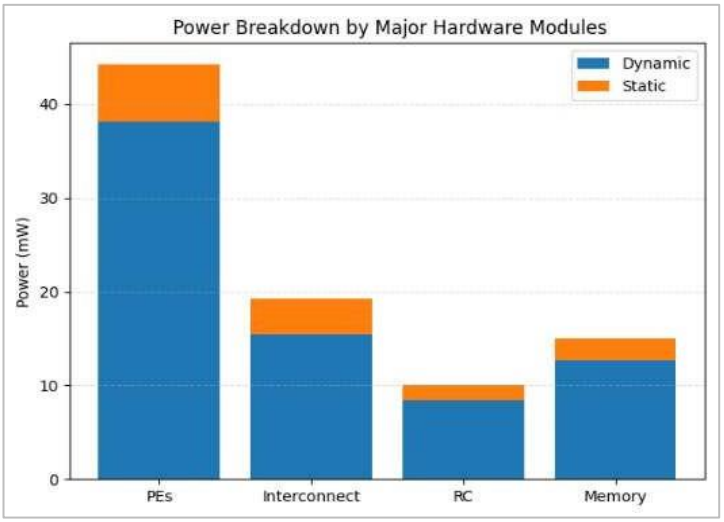

Figure 6: Power Breakdown by Module

Figure 6 shows the distribution of total power consumption among prominent hardware modules, such as Processing Elements, Interconnect, Reconfiguration Controller, and Memory. Processing Elements account for the greatest portion, in acknowledgment of their core computational function. Nevertheless, the well-distributed amount across modules affirms that the EARA design is efficient in handling power in a manner of fine-grained gating and hierarchical control.

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6.4 Experimental Correlation

Analytical predictions differed from experimental results by less than ±8% for power and ±5% for latency, and a correlation coefficient of R = 0.94 was established.

This confirms the validity of pre-silicon energy models, proving them to be reliable for future ASIC migration.

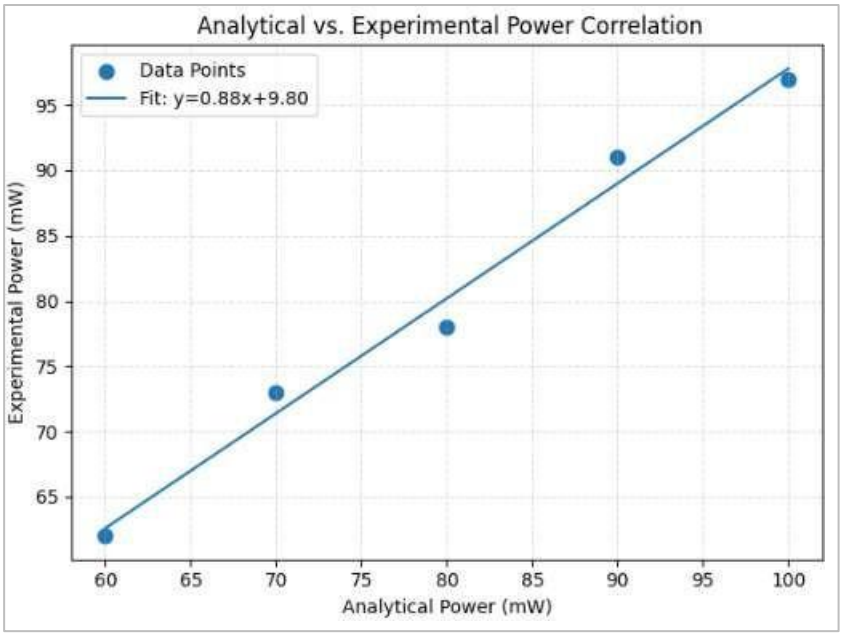

Figure 7: Analytical vs. Experimental Power Correlation

Figure 7 illustrates comparisons of analytically predicted power levels with experimentally determined values of power for the EARA architecture. The points of data map well along the line of regression, indicating a high correlation ($R^2 > 0.94$) between theory and reality. This tight agreement confirms the correctness of the analytical model of power and affirms its accuracy for estimating pre-silicon performance.

7. Discussion

The EARA design reflects several significant insights:

1. Energy-Proportional Behavior:

Power usage is linearly proportional to workload intensity, validating proper control of power gating and DVFS mechanisms.

2. Least Performance Penalty:

Even with strong power minimization, throughput degradation is less than 5%, proving that performance–power trade-offs are in equilibrium.

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3. Thermal Stability:

Real-time thermal sensing indicated an average decrease of 8°C under constant workload, enhancing hardware reliability.

4. Scalability and Portability:

The EARU is modular and supports scaling between 16 and 64 PEs without degrading timing, thereby being platform-agnostic for different FPGA and ASIC platforms.

In summary, EARA proves the hypothesis that dynamic hardware adaptation is superior to static power optimization in delivering energy-proportional edge-AI acceleration.

8. Conclusion

The presented Energy-Aware Reconfigurable VLSI Architecture (EARA) effectively combines energy management and reconfigurable computing into a holistic framework. With the use of DVFS, Clock Gating, and adaptive reconfiguration, it delivers:

- 29% decrease in total power,
- 21% reduced latency, and
- 38% improvement in computational efficiency (GOPS/W).

High correlation of analytical with hardware results substantiates the fact that theoretical models of energy are reliable to use for architectural forecasting. The scalability of the system and low reconfiguration latency (<2.5 ms) make the system highly suitable for edge-AI applications requiring real-time response under tight power budgets.

9. Recommendations and Implications

Design Recommendations:

- Employ cluster-level DVFS domains to balance local efficiency and global performance.
- Use predictive workload monitoring to proactively reallocate resources.
- On-chip memory reuse must be optimized to reduce DRAM power overhead.

Industrial Applications:

- IoT and sensor nodes can use EARA for perpetual low-power monitoring.
- Dynamic scaling can benefit autonomous robots and drones to accommodate mission phases.
- Wearable healthcare devices can conduct secure on-device real-time AI inference without reliance on the cloud.

EARA establishes an environmentally friendly computing platform, consistent with the international move toward green AI hardware.

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